REMARKS

Claims 1-26 are pending in this application. Claims 1, 3-6, 10-12, 16, 17, 20 and 21 have been amended to further define the invention. Claims 1, 3, and 4 have also been amended to overcome the rejections under 35 U.S.C. § 112. No new matter has been entered through these amendments.

Rejections under 35 U.S.C. § 102

Claims 1-16, 18-21, and 23-24 were rejected under 35 U.S.C. § 102 as being anticipated by US Patent 6,401,186 to Blodgett. In light of the amendments to claims 1, 6, 11, 16 and 21, Applicants respectfully request that these rejections be withdrawn.

Claim 1 has been amended to include the feature that the data associated with the second address is stored in the temporary data storage area according to most significant bits of a signal requesting the data associated with the second address. Applicants respectfully submit that Blodgett does not disclose this feature, as Blodgett requires comparison of the entire bit sequence and not a portion of the bit sequence, such as the most significant bits (see Blodgett, column 6, lines 13-21). Regarding the Examiner's statement that when the most significant bits are the same this is a hit, and when the most significant bits are different this is a miss, Applicants respectfully request that the Examiner specify where the most significant bits of the signal, or any portion of the signal rather than the entire bit sequence, is compared in Blodgett. Applicants respectfully request that the Examiner consider the claim language that specifies that the most significant bits are compared to determine whether to fetch the data from the main memory or the buffer, as Blodgett fails to disclose this feature.

In addition, Applicants would like to point out that claim 3 has been amended to specify that if the corresponding most significant bits are equal, then the data is accessed in the temporary data storage area according to the first and second least significant bits. Support for this feature may be found in Tables 1 and 2 and corresponding text of the application. Nowhere does Blodgett refer to using the least significant bits for locating any data. The Examiner refers to

column 6, line 62-column 7, line 8 of Blodgett with reference to this feature. This section refers to generating an address internally in the memory controller when a valid new address is not provided on the external address line (see column 6, lines 53-61). In the section cited by the Examiner, the most significant bit is incremented and the least significant bits are held constant in Table 1, while the most significant bit is incremented and the least significant bits are reset to 0,0 in Table 2. This is the prediction logic for generating new addresses to fetch from memory avoided by the embodiments of the present application. Applicants respectfully request that the Examiner specify how generating new addresses to fetch from main memory to place in a read cache discloses accessing a temporary data storage area according to first and second least significant bits. The least significant bits of the present application signify the location in the temporary storage area, while the individual least significant bits in Blodgett have nothing to do with the location in the temporary storage area. Accordingly, claims 1-5 are not anticipated by Blodgett for at least these reasons.

Claim 6, as amended, includes the features of determining if a next read command corresponds to the data associated with the consecutive address according to corresponding most significant bits of the read command and the next read command; and obtaining the data from the buffer according to least significant bits of the next read command if the next read command corresponds to the data associated with the consecutive address. As discussed above with reference to claim 1, Blodgett does not disclose these features, and instead requires the prediction logic avoided by the embodiments of the present invention. Applicants would also like to point out that claim 10 has been amended to include the feature that the data select signal corresponds to the least significant bits of the next read command. Blodgett fails to disclose this feature. Accordingly, claims 6-10 are not anticipated for at least these reasons.

Claim 11 has been amended to include the feature of logic for determining if a request for data associated with a next read operation is for the data associated with the consecutive address in the temporary storage according to corresponding most significant bits associated with requesting the read and the next read operation. As discussed above with reference to claim 1, Blodgett

requires comparison of the entire bit sequence and not corresponding most significant bits. Accordingly, claims 11-15 are not anticipated by Blodgett for at least these reasons.

Claim 16 has been amended to include the feature of circuitry configured to determine whether the second request is for the data associated with the consecutive address according to corresponding most significant bits associated with the first request and the second request. As discussed above with reference to claim 1, Blodgett requires comparison of the entire bit sequence and not corresponding most significant bits. Accordingly, claim 16 is not anticipated by Blodgett for at least these reasons.

Claim 21 has been amended to include the feature of a memory controller in communication with the read buffer, the memory controller configured to issue requests for one of fetching data in memory having an address associated with the read command and fetching data in memory associated with a consecutive address to the address according to least significant bits of the request for fetching data in memory. As discussed above, nowhere does Blodgett disclose using the least significant bits of a request to fetch data in memory. Blodgett discloses generating new addresses when new addresses are not provided by the microprocessor by resetting or holding the least significant bits constant, however, this is unrelated to the claimed invention. Accordingly, claims 21, and 23-24 are not anticipated by Blodgett for at least these reasons.

Rejections under 35 U.S.C. § 103

Claims 17 and 22 were rejected under 35 U.S.C. § 103 as being unpatentable over Blodgett in view of US Patent No. 6,507,899 to Oberlaender. Applicants respectfully disagree with the Examiner's characterization of Oberlaender. The two multiplexers referred to in Oberlaender in the cited section include one multiplexer 3 connected to an address buffer and one multiplexer 7 connected to a data buffer (see Figure 1 and column 1, lines 52-66). Claims 17 and 22, as exemplified in Figure 3, specify that the first and second multiplexers are coupled to the data buffer. Furthermore, claim 17 has been

amended to specify that the second multiplexer is not coupled to the RAM. In contrast, Oberlaender requires that multiplexers 7 and 8 be coupled to the RAM.

According to the Examiner one skilled in the art would be motivated to combine the references so that the reading instructions can be executed in one cycle. However, the Examiner states with regard to the rejection of claim 2 that Blodgett teaches obtaining the data in one clock cycle. Therefore, one skilled in the art would not add the multiplexers of Oberlaender to Blodgett as the added circuitry would only slow accesses down and could never speed the data accesses up. If the Examiner maintains this rejection, Applicants respectfully request that the Examiner explain how combining Blodgett and Oberlaender would make accesses faster than one clock cycle. Applicants respectfully submit that there is no motivation to combine the cited references as suggested by the Examiner.

Additionally, since claims 17 and 22 depend from independent claims 16 and 21, respectively, they are patentable over the cited combination for at least the same reasons as their respective independent claims, as Oberlaender fails to cure the deficiencies of Blodgett discussed above with references to claims 16 and 21. Accordingly, claims 17 and 22 are also patentable over the cited combination for the same reasons as their independent claims.

Claims 25 and 26 were rejected under 35 U.S.C. § 103 as being unpatentable over Blodgett in view of US Patent No. 6,920,488 to Le Pennec. Claims 25 and 26 depend from independent claim 21. Le Pennec fails to cure the deficiencies of Blodgett discussed above with references to claim 21. Accordingly, claims 25 and 26 are patentable over the cited combination for at least these reasons.

Conclusion

In view of the foregoing, Applicant respectfully submits that all of the pending claims are in condition for allowance. Favorable action is respectfully requested. In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at **(408) 952-6126**.

Respectfully submitted,

Michael T. Gabrik
Registration No. 32,896

Please address all correspondence to:

Epson Research and Development, Inc.
Intellectual Property Department
150 River Oaks Parkway, Suite 225
San Jose, CA 95134
Phone: (408) 952-6000
Facsimile: (408) 954-9058
Customer No. 20178

Date: January 6, 2006